

TESSOLVE

A **HERO ELECTRONIX** VENTURE

IC Design

IC Design and Engineering Services

Tessolve's IC team of 1250+ engineers provides complete Spec-to-GDSII solutions to our customers. Together with Tessolve's post-silicon engineering solutions, we provide end-to-end ASIC development services, enabling our customers to realize successful silicon.

IC Design /Technology Services Overview

- IC Design Solutions from "Specification to GDSII signoff" for Analog, Digital, and Mixed Signal chips across process nodes from 350nm down to advanced 3nm nodes for Automotive, data Center, AI and IoT applications.
- Digital Design Turnkey Capabilities – Architecture, RTL Design, Verification, DFT, Synthesis & STA, Physical design till GDSII signoff.
- Analog/AMS Design Turnkey Capabilities – Architecture, Circuit Design, Analog Modelling, Layout Design, AMS Verification.
- Robust Technical Program Management and Quality Processes to ensure first pass Silicon.
- In-house EDA tool licenses, compute infrastructure, flows and CAD support for turnkey program execution.



Our IC Capability

- **Analog & Mixed Signal**
- **RTL Design and FPGA Emulation & Validation**
- **Design Verification (DV)**
- **Design for Test (DFT)**
- **Physical Design**
- **Foundation IP Services**

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Analog & Mixed Signal (AMS) Design

The Analog and Mixed-signal design team at Tessolve specializes in High-quality design for different applications with process nodes varying from 350nm down to advanced 3nm nodes. The IPs were developed for various industry verticals like Automotive, Communication, Consumer, Medical, IoT, etc. The competent team has rich experience in delivering more than 70+ silicon-proven Analog chips during the last few years with full ownership of the delivery from Spec to GDSII signoff, supported with silicon validation to global semiconductor companies.

- Complete Analog Design life cycle from specs to post-silicon validation.
- Expertise in developing Full IP & Block level.
- Expertise in CMOS/FinFET process nodes: 3nm, 5nm, 7nm, 10nm, 14nm, 22nm, 45nm, 65nm, 90nm, 130nm, 180nm & 350nm.

RTL Design and FPGA Emulation & Valdation

Tessolve offers RTL design services from product specifications for both IP and SOC Development. Offerings include:

- Standard and Complex IP Block Design and Development.
- SoC and Sub-system Integration, Clock and Reset design, Clock gating, Low-power design, UPF definition.
- RTL Quality Checks: Lint, CDC, Automated property checks, Low-power checks.
- Protocol Experience: HSIO Protocols (PCIe, USB, MIPI), AMBA protocols (AXI/AHB/APB), Memory interfaces (DDRx/LPDDRx), Low-speed peripheral interfaces (I2C, SPI, UART, MDIO, I2S).
- Experience with the Xilinx & Intel FPGA device family.
- FPGA-based emulation, FPGA partitioning, ASIC to FPGA & FPGA to ASIC conversion.
- Custom board development and FPGA validation.

Design Verification

Verification is one of the most significant tasks in silicon development and has the most significant impact on the critical business drivers of quality, schedule, and cost. With its large pool of verification resources and investments in tools and verification methodologies, the customer is in safe hands to get all its validation needs to be addressed with Tessolve.

- IP and SOC-level Verification using C/C++, SV-UVM methodologies.
- CPU (ARM, RISC-V, Tensilica) processed based on Verification.
- Robust Verification planning to achieve Functional and Code Coverage goals.
- Power-aware verification.
- Gate-level simulations and regression management.
- Tools for verification productivity – Formal Verification, PSS.

Design For Test

Our team of Design for Testability experts can help with the chip DFT architecture and implementation to increase IC test coverage, yields, and quality. Coupled with our large ATE test team and infrastructure, we are uniquely placed to build a coherent strategy and implement DFT that improves the testability of the IC in the post-silicon phase for first-pass silicon. Tessolve's DFT service offerings include the following:

- DFT architecture and scan methodology.
- RTL-level DFT quality checks.
- Scan insertion, ATPG pattern generation, and Verification.
- Memory BIST and Boundary Scan.
- Fault Coverage Analysis, Debug, and Improvement.
- Post-silicon debug support.

Physical Design

Tessolve's physical implementation services include:

- Executed multiple Mixed Signal SOCs from spec to silicon in parallel.
- Specialized in complex IP's and subsystems in Graphics, Processors, PCIE-Gen5, CXL3.0, GDDR6, LPDDR4, and Automotive domains.
- Timing closure of high frequency designs up to 3Ghz and technology down to 3nm.
- Development of complex Low Power SPEC & Implementation.
- Development of Timing, Sign off Specs and comprehensive checklists.
- 250+ PD professionals.

Foundation IP Services

- PDK development and qualification services
- Memory design, char and layout services
- Standard cell design, char and layout services

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