

TESSOLVE

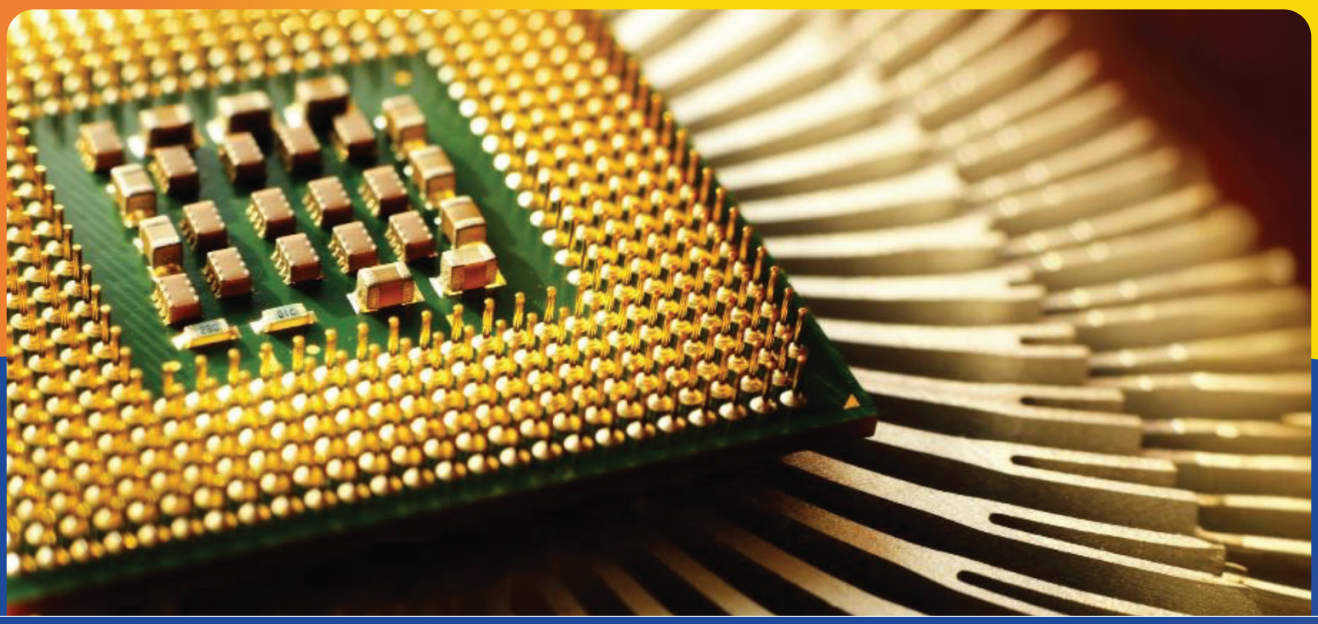
A **HERO ELECTRONIX** VENTURE

Design Verification Services

Improving quality whilst reducing costs and TTM

- With increasing design complexity, Pre-silicon Verification continues to consume the largest engineering effort in silicon and has the biggest impact on the key business drivers of quality, schedule, and cost.

- Tessolve brings verification expertise across multiple industry verticals spanning Consumer Electronics, Industrial, Wireless, Data Centre/Enterprise, Automotive and Storage segments.



Tessolve verification offerings cover all aspects of the Verification flow from feature extraction to coverage closure and is equipped with custom-designed verification productivity tools for reducing verification turnaround times.

Verification Plan

- Traceability to specifications
- Test Scenario Plan
- Checker Plan
- Functional Coverage Plan

IP/Block Verification

- Full IP level verification
- IP fully trusted at SoC level
- Mixed-signal verification

SOC Verification

- Reuse of IP Level test cases
- Connectivity
- Integration
- Use-case
- Regression Management

Functional & Code Coverage

- Fully meet Functional & Code Coverage targets
- Predictable time & resources to finish

Gate Level Simulations

- Prioritization of verification scenarios
- Efficient RTL-Netlist hybrid simulations

Tapeout to Fab

AI-Assisted Verification and Debug

EDA, Compute, Storage

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Tessolve's Design Verification Expertise and Scale

Expertise

- IP Verification
- SOC Verification
- CPU/GPU Verification
- DFX Validation
- Mixed signal verification
- Display and Video Sub-system Verification
- Low-power RTL and Netlist verification
- Gate Level Simulations

Scale

~450 Engineers across:

- IP
- SS/SOC
- GLS
- DFX

Methodologies

- SV-UVM; C/C++ ; Vmanager
- Formal Verification
- PSS – Portable Stimulus standards
- AI/ML Assisted Verification

Low-speed peripherals

- SPI/QSPI
- I2C/I3C
- I2S
- UART
- CAN 1.0/2.0
- SPDIF

Memory interfaces

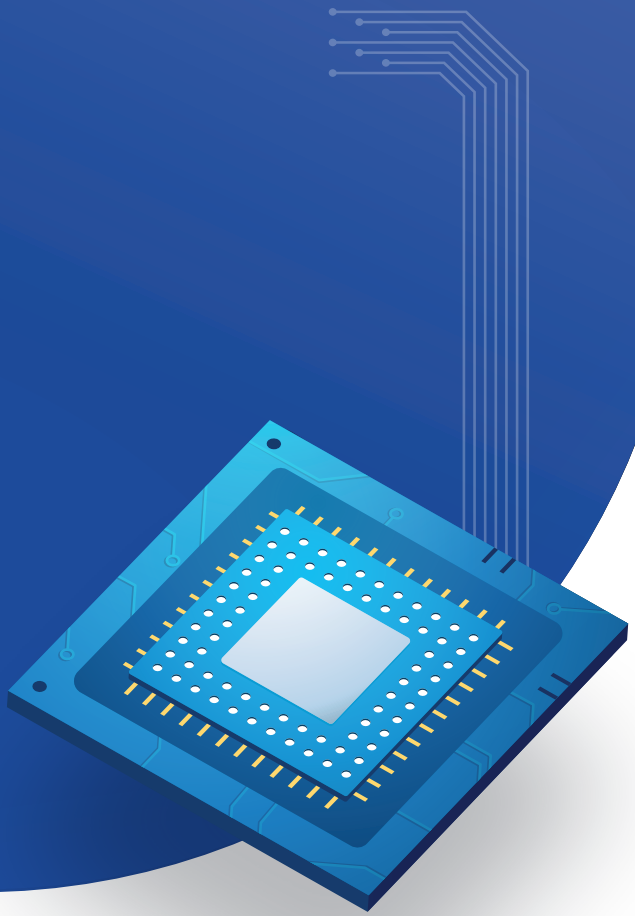
- SD Card 3.0
- ONFI 3.2
- LPDDR/DDR 3/4/5
- UFS
- NVMe

CPU Core & Infra

- CPU: ARM Cortex A*, M*; RISC-V; Tensilica
- SOC Interconnects: Arteris FlexNOC, ARM -CMN, CCI, NIC,
- AMBA protocols – AXI, ACE, CHI, AHB, APB
- ARM Coresight debug

HSIO

- Ethernet 100/1G/10G
- PCIe GEN 3/4/5/6
- UCIe 1.0/1.1/2.0
- USB 2/3
- SPI 4.2
- DP 1.2
  MIPI - DSI, CSI, D-PHY, C-PHY



Tessolve's DV Value Proposition

- Improved effective, efficient verification
- Improve quality
- Formal Verification
- Reduce costs
- Improve time-to-market



Value-adds

Formal Verification
- Development of a Formal Verification Strategy
- Full Formal Verification of complex IP Blocks
- Automate checks at SoC level
  Connectivity, X propagation, power checks, etc

AI/ML Assisted-Verification
AI assisted Spec to feature analysis
Automated TB generation from feature extraction
ML support for coverage closure

Verification Consultancy
- Audit current verification practices across the organization
- Identify and agree potential improvements
- Establish low overhead, best-in-calls verification processes

Recent Successful Verification Projects

Chip Application	Design Complexity & Key Blocks	Tessolve's DV Scope
5G Communication SOC	• Multi-core RISC-V Sub-system • Multi-core Tensilica based • Real-time Sub-system • Multi-core DSP Subsystem • LPDDR4 Memory Subsystem • Other interfaces: • 25G Ethernet SERDES, USB2, Low-speed peripherals, AFE	• SOC Testbench Architecture Definition & Development from scratch • SOC Test plan development • Test case coding, Verification, Regression, & Coverage Closure • Performance DV test bench Arch Definition & Development • Performance Verification test plan, coding, verification & Correlation • Gate-level Simulation (Zero-delay & timing)
Automotive chip for Autonomous vehicles	Multi-CPU ARM-based MCU, Application Processing and System Control Clusters MMU FlexNOC-4 LPDDR5 Memory interface HSIOs: PCIe GEN6, UCIe 1.0,USB3, USB3, Display Port 1.4	• Functional Safety Verification – FUSA • Checking that errors in memory will cause interrupt, reset or chip output notification • SOC Test plan development • SV/UVM based Testbench development at Unit level • Porting of ASM testcases • Assertion implementation • Pin Muxing • X-Prop Simulation • Save and Restore • Test case coding, Verification, Regression, & Coverage Closure • Performance Verification test plan, coding, verification& Correlation